SID2H technical description

Optical system

Beam shaping optics

The beam shaping optics, shown in figure 1, are contained in the angled laser delivery tube. Light from a 100mW, 532nm Nd-YAG laser is directed down the centre of the tube and first passes through a 532nm zero order quarter wave plate (QWP), which converts the linearly polarized output of the laser to circular polarization. After the QWP there is a plano-concave lens that causes the beam to diverge, and then a cylindrical lens to focus the light in one dimension at the scattering volume position. Near the end of the tube is a flat mirror to fold the beam so it is orthogonal to the airflow. Thus the beam is approximately 3mm wide and 140μm deep at the scattering volume.

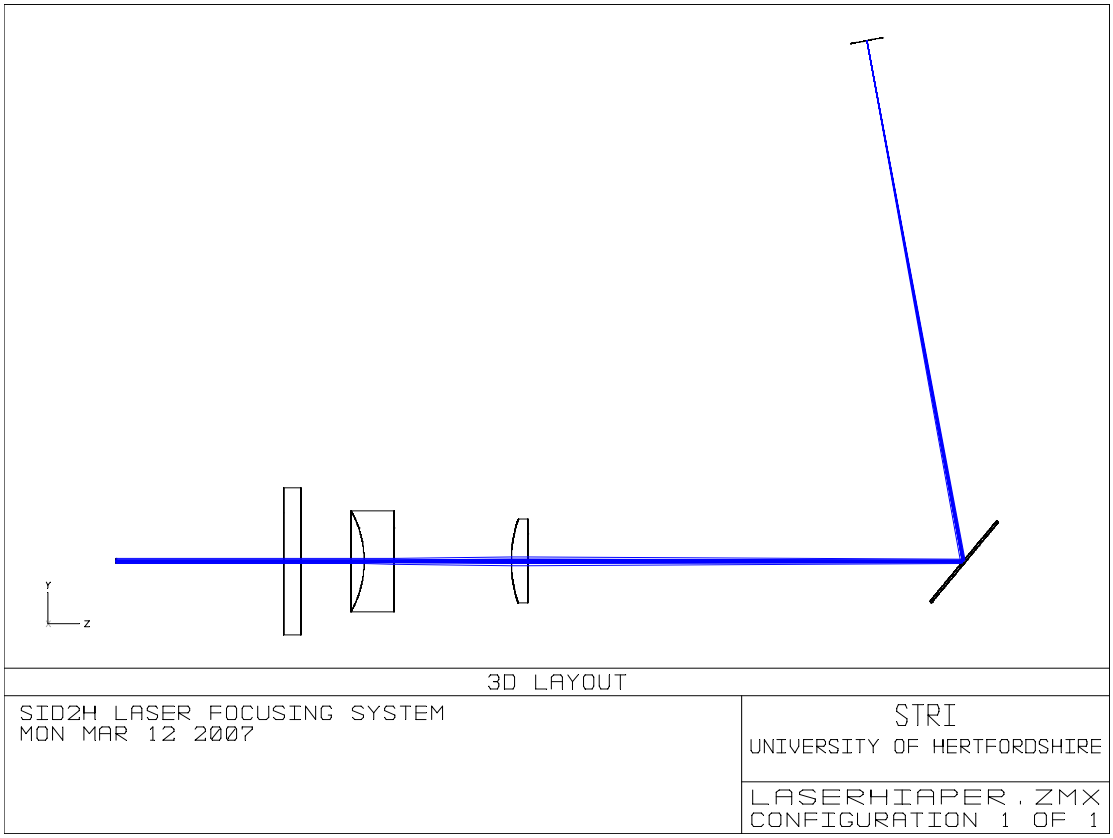

Figure 1. Beam shaping optics.

Trigger optics

The trigger optics, shown in figure 2, are imaging systems which image an area of the laser beam onto a PMT detector. The trigger optic tubes are arranged at a scattering angle of 45° with respect to the laser, and cover a half angle of 9.3°. Light from the scattering volume first passes through a sapphire window and then an achromatic lens that collimates the light. The light then impinges on a 532nm bandpass filter with a bandwidth of 10nm that minimises changes in signal level due to ambient light. Finally a second achromatic lens focuses the light. At the focus there is an iris, the size of which defines the size of the scattering volume. For the small volume trigger this is 0.3mm diameter and for the large 0.6mm diameter. Behind the iris the light falls on the faceplate of a TO8 can PMT with a 8mm diameter input window, producing a current pulse when a particle is in the scattering volume.

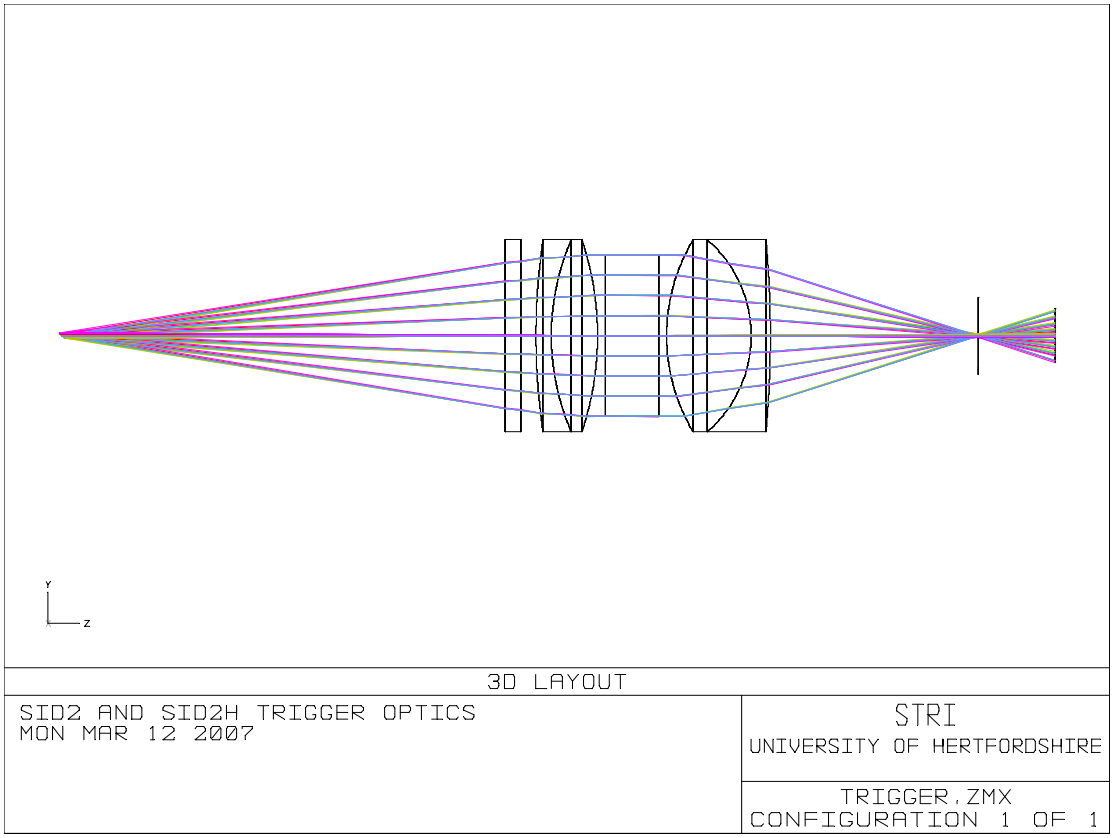

Figure 2. Trigger optics

Main optics

The main optic system, shown in figure 3, is a Fourier transform system which maps scattering angles to positions on the imaging plane. It is centred on a scattering angle of 0° and has a half angle of 20°. Light from the scattering volume first passes through a sapphire window and then two plano-convex lenses that collimate the light onto a 532nm bandpass filter with a bandwidth of 10nm. Light from the laser beam itself is prevented from entering the optics by a beam dump on the sapphire window. After the filter a plano-convex lens brings the light to a pseudo-focus, then it passes through a double-convex correcting lens before falling on the input faceplate of a fibre optic relay. At the pseudo-focus is an aperture that reduces background light from the beam. Between the focusing lens and the correcting lens is a flat folding mirror. The fibre relay transfers the light onto the faceplate of a 32 element multi-anode PMT. The relay consists of 28 groups of 9 fibres each, arranged at the input end in an annulus of 28 sectors. The output has a rectangular arrangement of 28 rows of 9 fibres each, hence only 28 of the 32 elements of the PMT are used.

Electronics

Overview

The connectivity between the various PCBs of the SID2H system is shown in figure 4. The system runs from a single PSU supplying 5V and +/- 12V. The laser is a self contained unit that runs from 12V. The rest of the system is controlled by the FPGA system controller which is located on the backplane of the electronics module. The individual boards are described in the following sections.

Trigger amplifier boards

Each trigger PMT has an amplifier board mounted alongside the trigger tube. Each board has a single op-amp configured in trans-impedance amplifier mode with a bandwidth of 1.9MHz. The outputs of the amplifiers are fed into the signal conditioning boards via coax cable.

Multi-anode PMT board

The multi-anode PMT board consists of the PMT itself, the HV PMT power supply and 28 trans-impedance amplifier op-amps, one for each of the 28 active channels. The amplifiers have a bandwidth of 1.9MHz and the outputs are fed into the signal conditioning boards via coax cables. The voltage of the power supply can be set via the miscellaneous board described later.

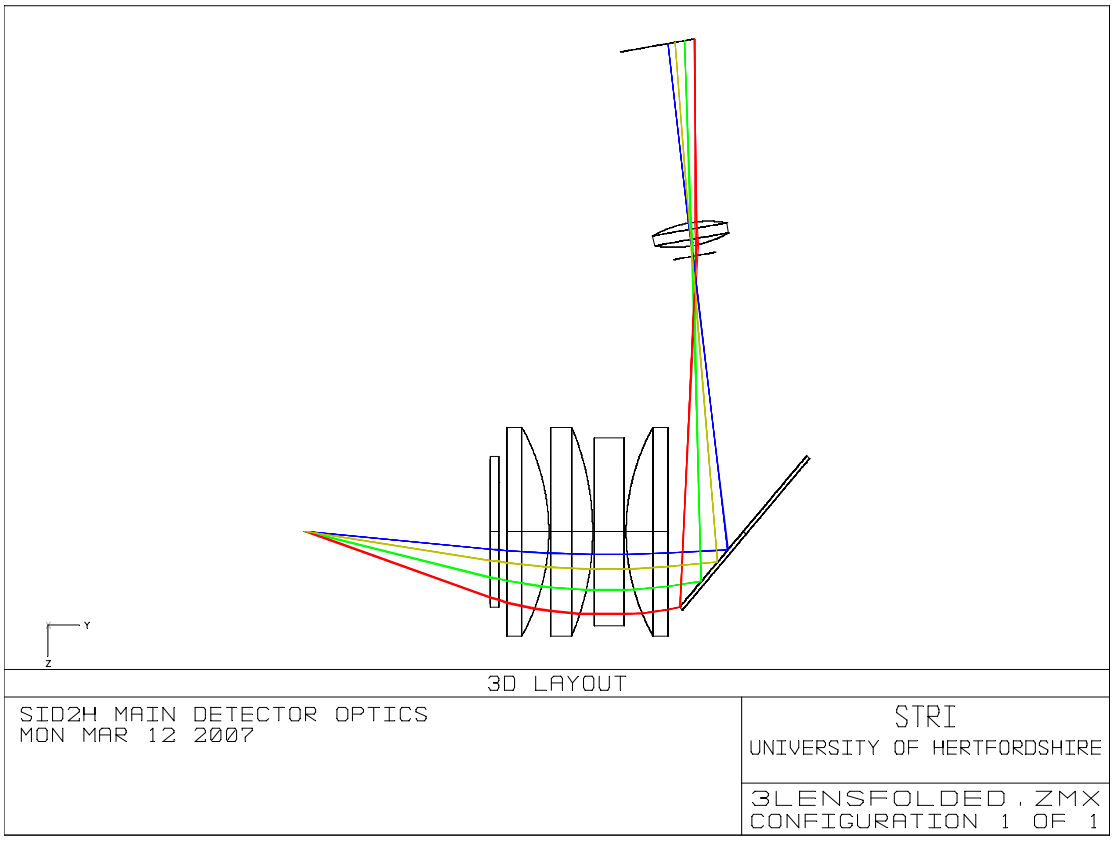

Figure 3. Main optics

Signal conditioning boards

SID2H has four signal conditioning boards, each with 8 channels, for a total of 32 channels. 28 channels are used for the 28 outputs of the multi-anode PMT board, two channels are used for the two triggers, and the other two are used for sensor (temperature and laser power) inputs.

Each of the eight channels on a board consists of a dc restoration circuit and a peak detector/integrator circuit. The channels are populated differently depending on the input type, as detailed below. Each board also has two 4-input, 12-bit ADCs that are used to digitise the signals from the eight channels. Each ADC has four registers which, after a conversion, hold the digitised values from its four respective channels. After conversion, an internal pointer is set to the first register and the data output on the ADC data bus. After a read the pointer is automatically incremented to the next value so the four data are obtained by four successive reads. Both ADCs are read simultaneously using a 24-bit data bus under the control of the backplane FPGA described later.

The dc restoration circuit is designed to bring the quiescent level (i.e. no particle present) of the signal to zero volts. The dc background level is made up of two components, stray light from the laser and a variable amount of ambient light depending on flying conditions. These together cause a dc offset of approximately 200-300mV which can vary by up to a few tens of mV. The dc restoration brings the background level to 0V, and maintains this by tracking slowly varying ambient light changes.

The circuit is shown in figure 5. This shows the configuration for negative going pulses, but in SID2H the pulses are positive going so the diodes are reversed and R1 is not fitted. Also not fitted are R13 and R14, which are used for a positive going pulse output. When no pulse is present, C1 is continually

trying to charge up to the supply rail via R132, but is prevented from doing so by U1 via D17. C1 is buffered by U2 and the output fed back to U1 so that the voltage on C1 is the same as the input. When a pulse is present the output of U1 follows the pulse and D17 becomes reverse biased, so C1 starts to charge. The time constant (1s) is such that the voltage on C1 changes negligibly for pulses of a few μs. After the pulse D17 starts to conduct again and discharges C1 until the voltages match. During the pulse D1 provides feedback for U1 to prevent it going into saturation. The voltage on C1 can follow slowly varying changes such as those produced by ambient light. The dc level from U2 is then subtracted from the input by U3, which is set up as a common mode rejection amplifier.

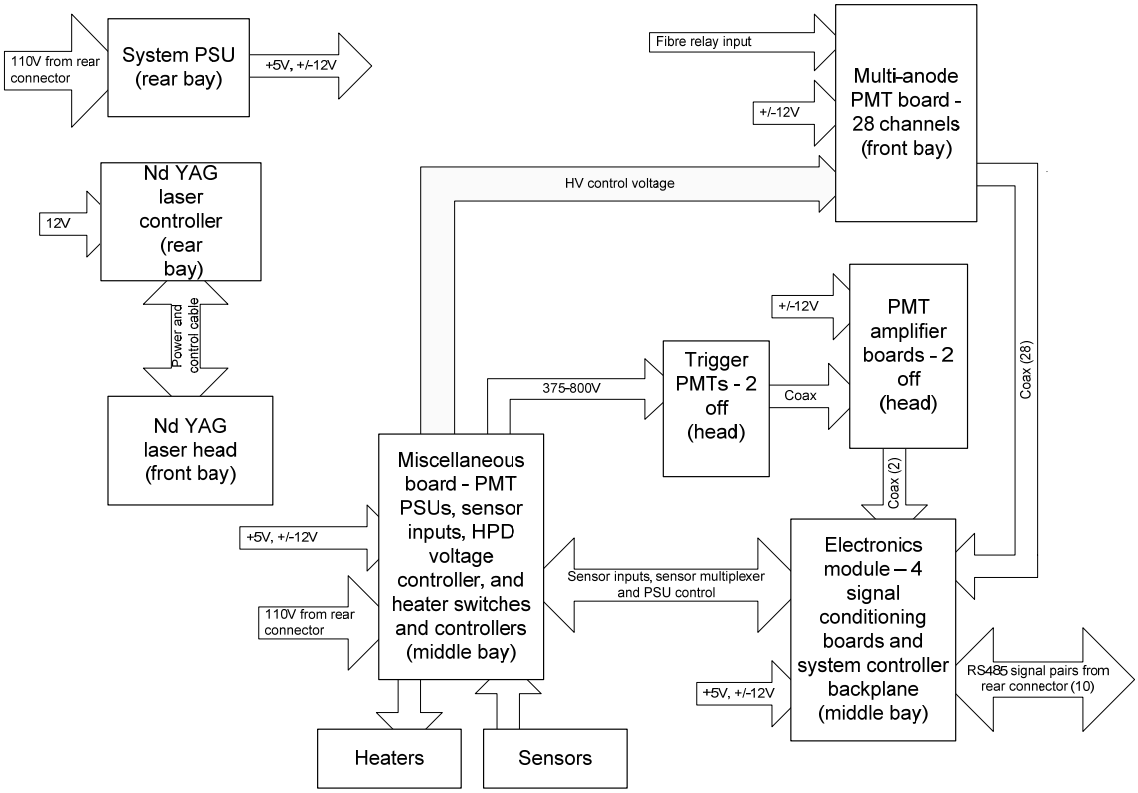

Figure 4. Electrical connectivity.

After the dc restoration, the signals enter a peak detection/integrator circuit. For SID2H this is set up in integrator configuration using only U4 and associated components as detailed in figure 5 and on the schematics. The reset and hold switches are controlled by the backplane PCB. While waiting for a particle event, the integrator is held in reset by the FPGA, so the capacitor C4 is prevented from charging. When the FPGA is triggered by pulses from the trigger boards, the integrator is taken out of hold and charge collects on the capacitor. At the end of a pulse the hold is asserted which breaks the signal path and prevents further charge accumulation. The output of the integrator is then digitised, after which the hold is de-asserted and the circuit put back into the reset state.

On channel 1 of the boards the input and dc signals are routed both to the subtraction amplifier and a comparator, which is used to provide a TTL trigger for the FPGA. This is set up for positive input signals and produces a negative going output. The trigger signals are connected to these channels on boards 1 and 2 of the system. For the trigger inputs the integrator is not fitted since digitising these inputs is not meaningful.

The inputs of channel 1 on boards 3 and 4 are the buffered outputs from temperature and laser power sensors. For these channels only the subtraction amplifier is fitted, with the inverting input tied to ground.

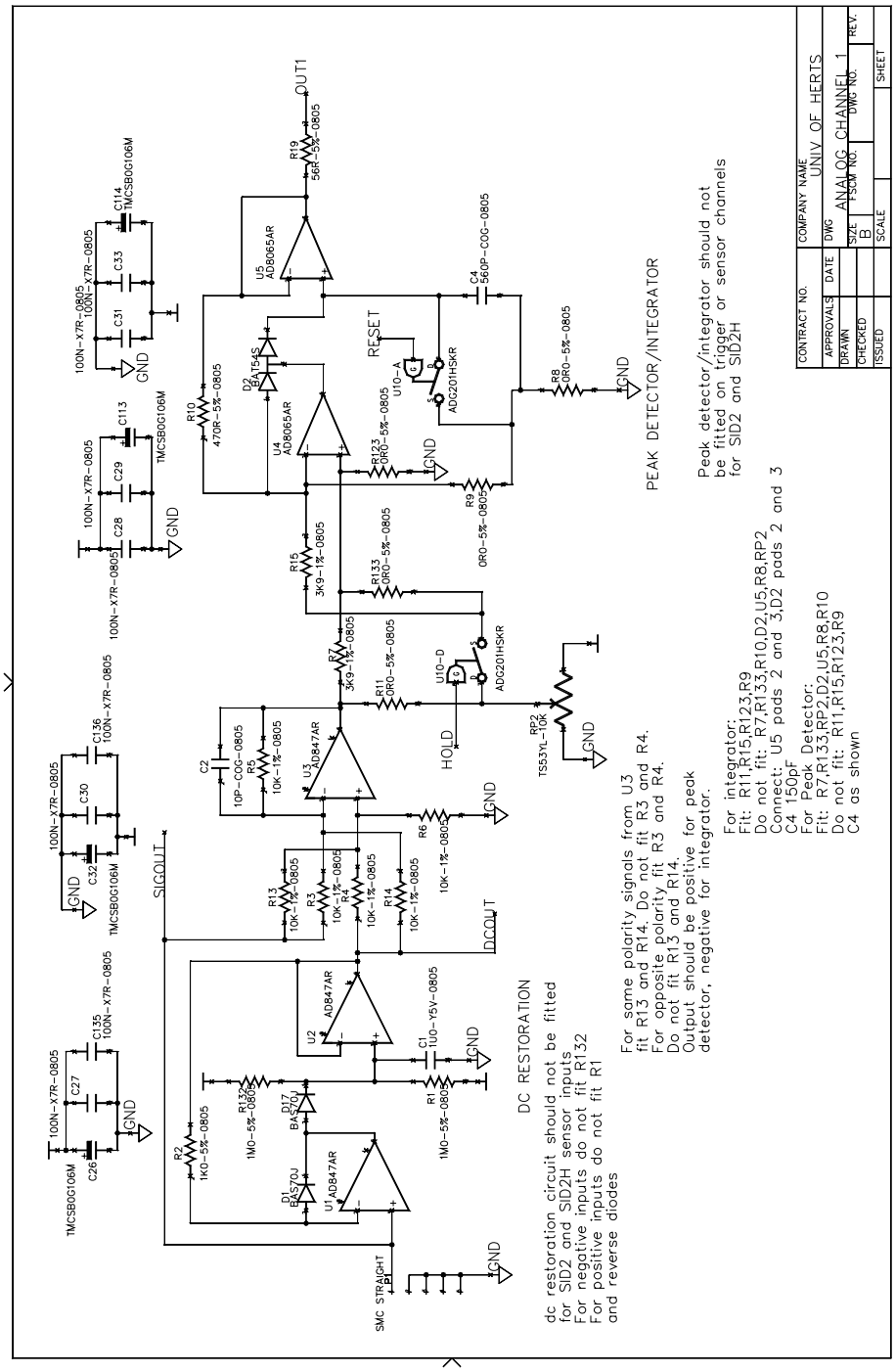

Figure 5. Channel 1 of the signal conditioning board.

Backplane board

The backplane consists of the system controller FPGA, 4 slots for interfacing to the signal conditioning boards, and RS422/485 drivers and receivers for transmission to/from the inboard computer. The FPGA controls all the functions of the probe, which comprise capturing, digitising and transmitting the data on occurrence of a particle event, periodic sending of data when no particles are detected and writing to the digital potentiometers that set the HV PMT supplies. Transmission between the probe and the inboard computer is accomplished using 10 RS422 data pairs. 7 pairs are used to send data from the probe to the computer, the other three used to send data in the other direction. In both directions one signal pair carries a clock and a second carries a synchronisation pulse to signify the

start of the data. The remaining pairs are data, five from probe to computer and one in the other direction.

Figure 6 shows a timing diagram of the digital sequence when a valid particle event occurs, which is signified by simultaneous negative going pulses on trigger_l and trigger_s. The pulse is first integrated as described previously, the control signals being int_rst and int_hld.

An AD conversion is initiated immediately after the hold is asserted by ad_conv. Conversion takes 7μs, after which the data is read from the ADCs. The reads are accomplished by ad_rd and ad_cs (0-3).

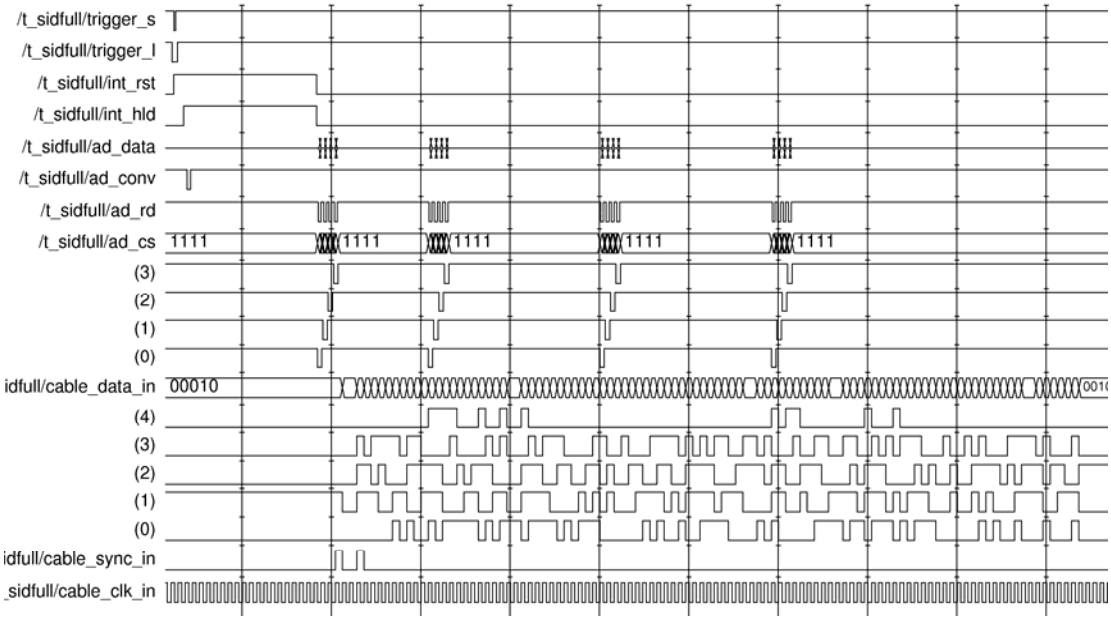

Figure 6. PFGA timing diagram for data capture and transmission.

The first ADC register value from each board is read sequentially and the data stored in four 24-bit registers in the FPGA. This process can be seen in figure 5 with the staggered ad_cs lines. These data are then shifted out serially on the four data lines (cable_data_in (0-3)), one for each board. A fifth line (cable_data_in (4)) carries timing data (system count, time of flight, etc). During the shift the second ADC register values are obtained by reading the boards sequentially again, the outputs being stored in the FPGA. When the first values have been shifted out the second values start to shift out and then the process repeats until four reads and shifts are finished. At the start of the shifting process a sync pattern is output on the sync line (cable_sync_in) so the receiver can sync to the start of the data.
The FPGA also computes a 24-bit CRC as the data is being shifted out. This is tagged onto the end of the data and shifted out, split over the four data lines cable_data_in (0-3).

Miscellaneous board

The miscellaneous board has three functions. Firstly, the PMT power supplies for the two trigger PMTs are mounted on this board. The voltages of the power supplies are set by digital potentiometers controlled by the FPGA, and a third potentiometer sets the voltage of the power supply on the multi-anode PMT board. All three are written together when a bit in the data stream to the probe is set. This is accomplished by writing to a register on the DSP Omnibus board. Figure 7 shows an example of writing to the potentiometers. Cable_clk_out, cable_sync_out and cable_data_out are the three wire pairs from the computer. The FPGA detects if the relevant bit in the data stream is set and if so writes the data to the potentiometers on pot_dq, first enabling the write by setting pot_rst high.

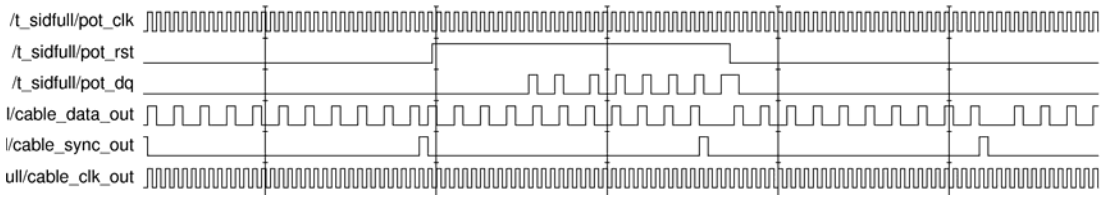

Figure 7. Timing diagram for writing to the digital potentiometers.

The second function of this board is to interface to the laser power monitor and the seven temperature sensors. The sensors are connected to the inputs of a 16:1 multiplexer. The output of the multiplexer is switched to a different sensor by the FPGA every time a particle event occurs, and also every 0.4s approximately when no particles are present. The multiplexer output is buffered and then fed into channel 1 of signal conditioning board number 4. The sensor output is then digitised and transmitted along with the particle data. In addition the temperature sensor in contact with the multi-anode PMT is buffered and connected to channel 1 of signal conditioning board number 3 so its value is available with every particle.

The third function is control of the heaters. In addition to being connected to the multiplexers, three of the temperature sensors, the laser, the laser controller and the optics heater sensors are connected to comparators that switch when the temperature is approximately 5°. The buffered outputs of these drive solid state relays that switch the 110V ac power to resistive heaters. For the laser and controller these are 100ohm resistors, for the optics heaters these are thermofoil heaters.

Omnibus card

The Omnibus card is the interface card between the RS422 transmission wiring and the DSP card in the computer. It is a daughter board mounted on the DSP card, interfacing to it through Omnibus site 1. The board has two FPGAs and two 8k by 16-bit FIFOs, and RS422 drivers. The FIFOs are wired in parallel to give a 32-bit word.

The receiver FPGA is responsible for collecting the data from the probe and writing it to the FIFOs. It takes its clock from the cable_clk_in signal, and monitors the signal cable_sync_in for the start of a particle data set. When this is detected the data on the five cable_data_in signals is shifted into five 24-bit registers and written to the FIFOs each time the registers become full. A total of 21, 30-bit words are written, which comprise a complete particle data set. Each word consists of 24 bits of particle data, and a 6-bit incremental count so the software can identify the data. The data format is detailed in the document ‘Software interface V1.0’. The FIFO full and almost empty flags are monitored by the FPGA. If the FIFOs become full then the FPGA stops writing data to them, and only resumes when the almost empty flag is set.

The Omnibus FPGA is the interface between the Omnibus interface on the DSP card and the FIFOs. It contains two read only and one write only registers, data, status and control respectively. These are also detailed in the document ‘Software interface V1.0’. When a read data instruction is received from the Omnibus interface it enables the FIFO onto the Omnibus data bus, and also tags on the FIFO full and empty flags in bits positions 30 and 31 so the software doesn’t have to read the status register on each data read. All the FIFO status flags are separately available by reading the status register. In addition the FPGA generates the cable_clk_out, cable_sync_out and cable_data_out command signals to the probe. Data to be sent out on these lines are written to the control register of the FPGA.