

Airborne Polarimetric Doppler Weather Radar: Possible Beam Forming Architectures

Jothiram Vivekanandan, Eric Loew, Adam Karboski and Bernard Hwang
Earth Observing Laboratory, National Center for Atmospheric Research, Boulder, CO 80301
vivek@ucar.edu

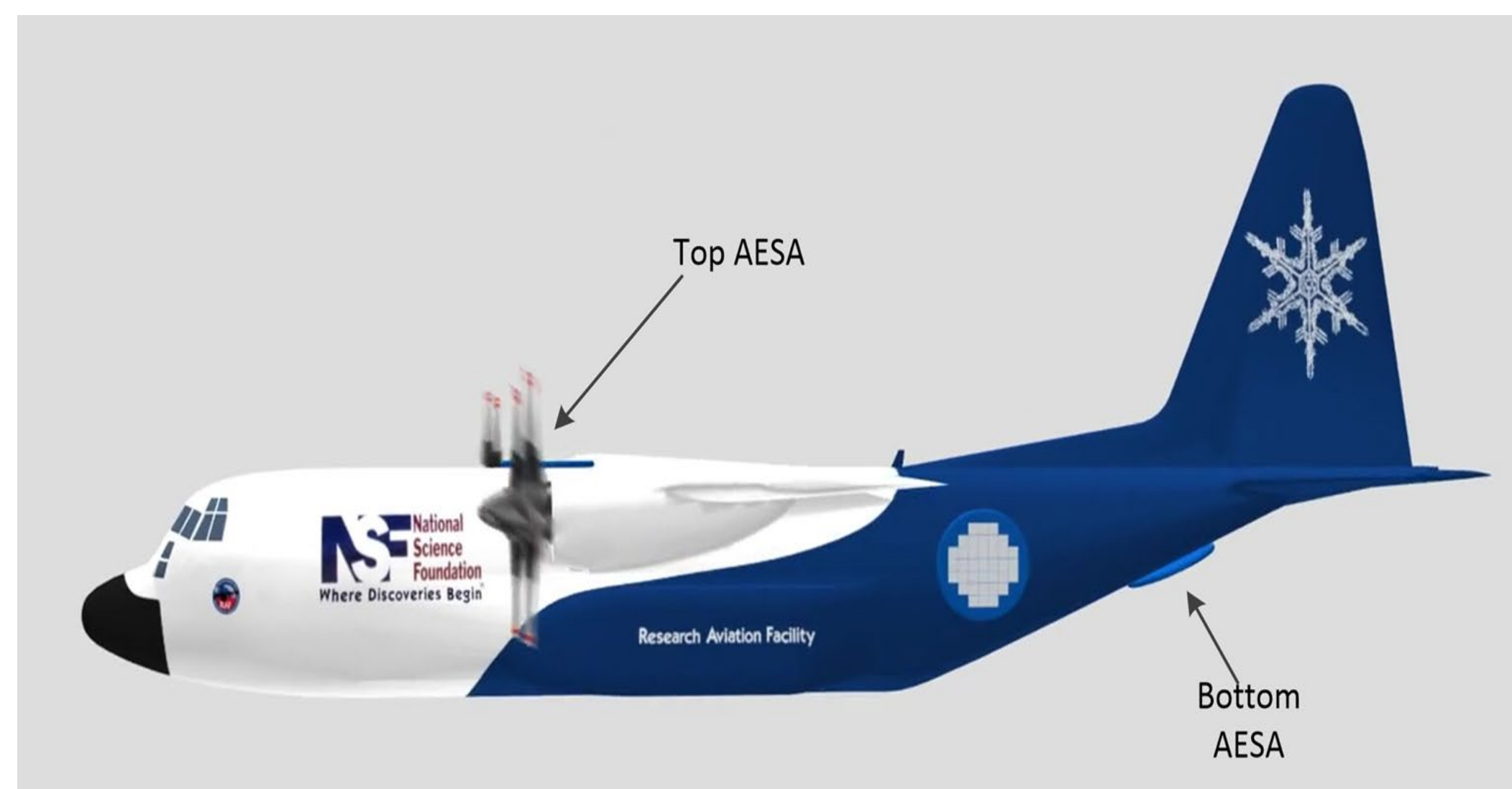
Introduction

The Airborne Phased Array Radar (APAR) with dual-polarimetric and dual-Doppler capability enables concurrent estimates of microphysical properties (e.g., precipitation types and sizes, quantitative precipitation estimation) and 3-D winds in precipitation (Vivekanandan et al. 2014). At present, no other airborne instrument has the potential to estimate 3-D winds and microphysics concurrently. The APAR will capitalize on Active Electronic Scanning Array (AESA) technology to incorporate beam multiplexing (BMX) mode of operation which is capable of collecting the desired number of samples, allowing more accurate radar measurements, in less time than a continuous sampling mode (Vivekanandan et al., 2018).

Phased array radar beamformers could be distinctly configured in three types of architecture: (i) analog, (ii) hybrid, i.e., a combination of analog and digital, and (iii) digital (Herd and Conway, 2016). These architectures, as they relate to the APAR requirements, are explored.

A notional phased array radar (PAR) of 37 panels of 8 X 8 element, line replace units (LRU) was considered for this study. A total of 2368 elements, each producing 4W peak power over a 7.5% duty cycle, and arranged in an alternating transmit, alternating receive (ATAR) architecture was assumed. Power consumption estimates were based on measured data from a 64 element LRU technology demonstrator prototype.

1. What is APAR?



Notional drawing of APAR AESA antenna panel placement on the C130. There are two side panels on port and starboard of the fuselage aft of the rear personnel doors.

APAR is a modular, dual-polarized, two-dimensional (2-D) electronically scanned C-band airborne phased array radar. It is currently in early development by the National Center for Atmospheric Research (NCAR). APAR will be capable of retrieving dynamic and microphysical characteristics of clouds and precipitation. The design of the NCAR APAR envisions it being flown on the National Science Foundation (NSF) NCAR C-130, operated by NCAR on behalf of NSF. The AESA is constrained within 70" diameter of C-130 fuselage as shown in the above figure. There is the potential for APAR to be flown on other C-130 aircraft (e.g. U.S. Hurricane Hunters and similar international research aircraft) for hurricane reconnaissance and monitoring high impact weather. APAR is intended to replace NCAR's ELDORA/ASTRAIA (Electra Doppler Radar/Analyses Stereoscopic par Impulsions Aeroport).

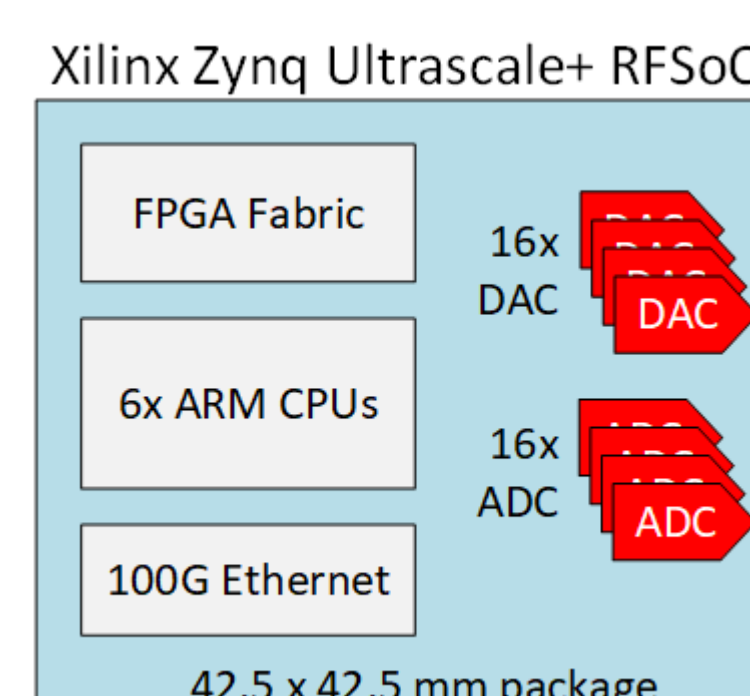
Parameter	Numeric value
Operating Frequency	C-band: 5.35 - 5.45 GHz
Antenna Aperture (maximum)	Fit within 70" diameter circle
Maximum panel thickness	<= 9 inches
Maximum weight for each AESA	<= 450 pounds
-3dB Beamwidth	< 2.2° (broadside on Tx)
Sensitivity	-11 dBZ at 10 km with 0 dB SNR
Reflectivity Variance	<1 dB
Doppler Velocity Variance	< 1 m/s
Produce full polarimetric matrix	Z, V, W, Z _{DR} , LDR, φ _{DP} , ρ _{HV}
Calibrated Z _{DR} for particle shape and QPE	Z _{DR} <= 0.2 dB
Differentiate liquid and ice	LDR < -22 dB
Differentiate melting	LDR < -27 dB
Polarization Tx and Rx	H or V linear

Table 1 Technical Specification of APAR

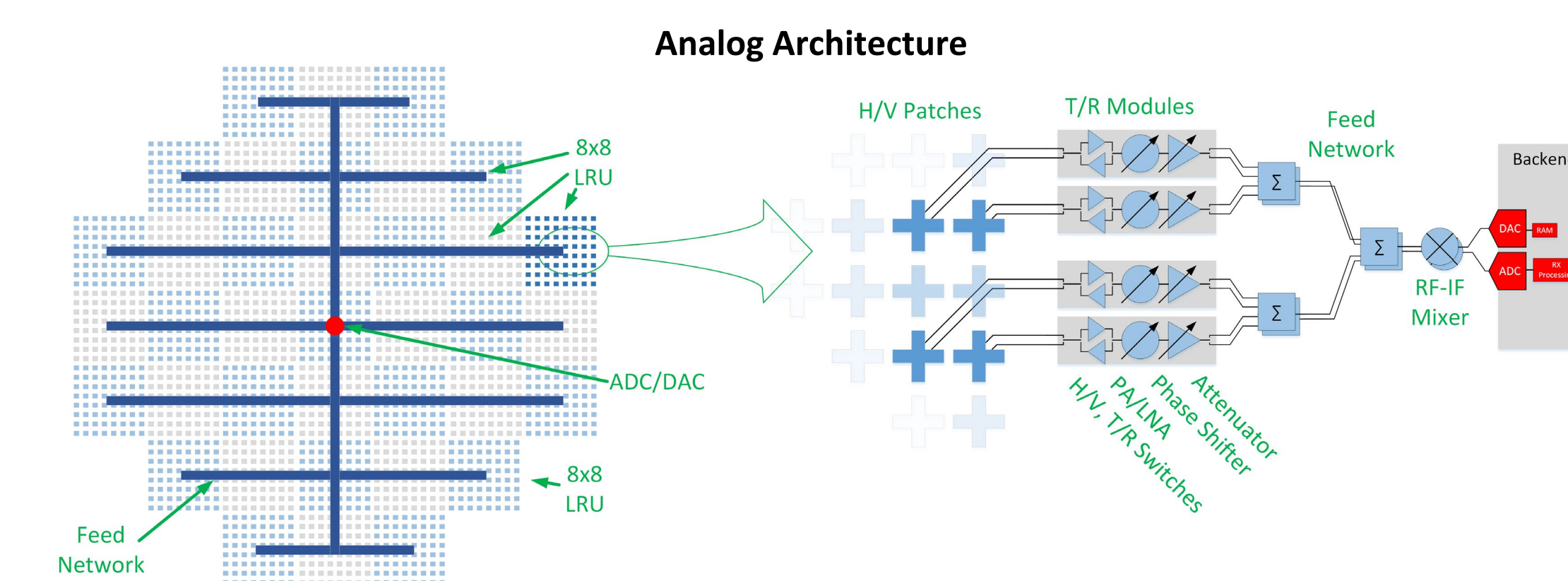
2. Digital Beamformer Enabling Technology - RFSoc

The Radio-Frequency System on Chip (RFSoc) is a disruptive technology which integrates Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) together with processing resources such as Field Programmable Gate Array (FPGA) fabric, on a single integrated circuit (Fagan et al., 2018).

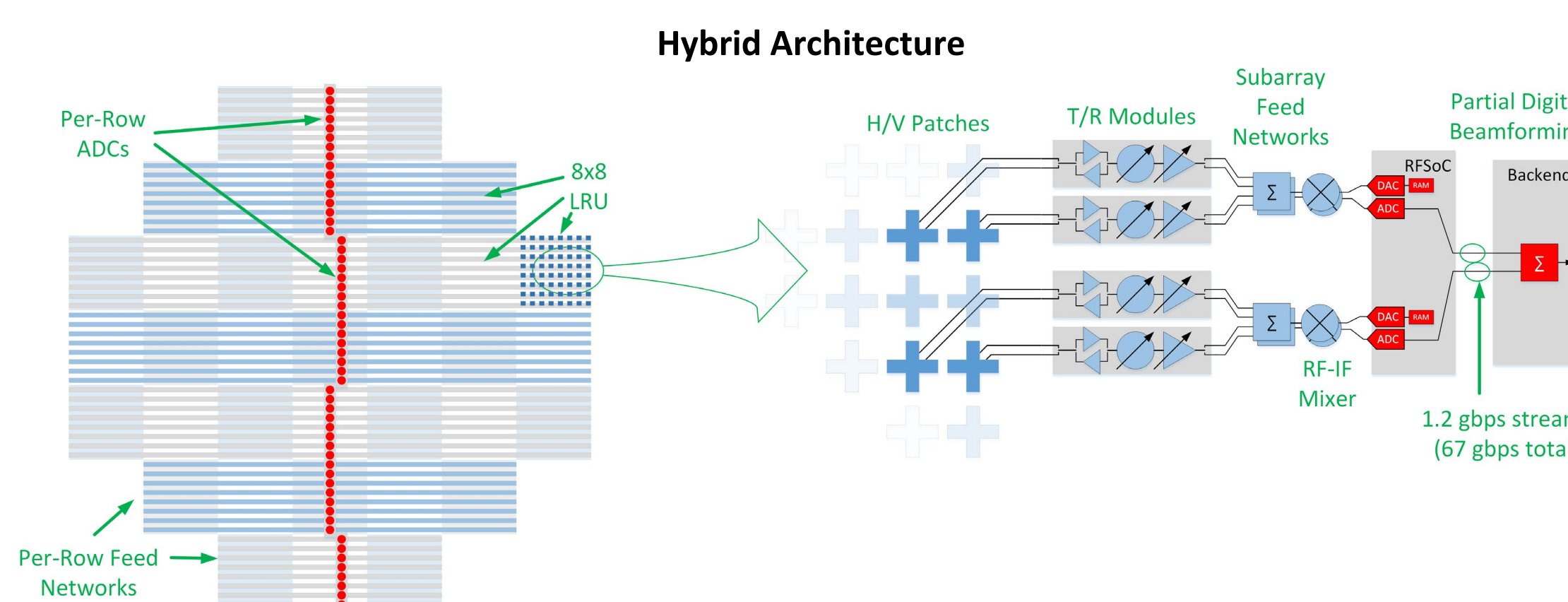
In a traditional system, digitizing a large number of channels requires an equally large number of interfaces between the processing chips and the ADC/DAC chips. The power consumption of the interfaces alone is prohibitive for an element-level digital architecture such as the one under consideration. By integrating multiple ADC and DAC channels into the FPGA/SoC device, a footprint reduction of 50% and a power reduction of 75% are achievable. The Xilinx Zynq RFSoc integrates up to 16 ADCs and DACs, together with sufficient processing resources and high-speed serial interconnect to implement the frontend signal processing and digital beamforming aspects of a phased array radar system.



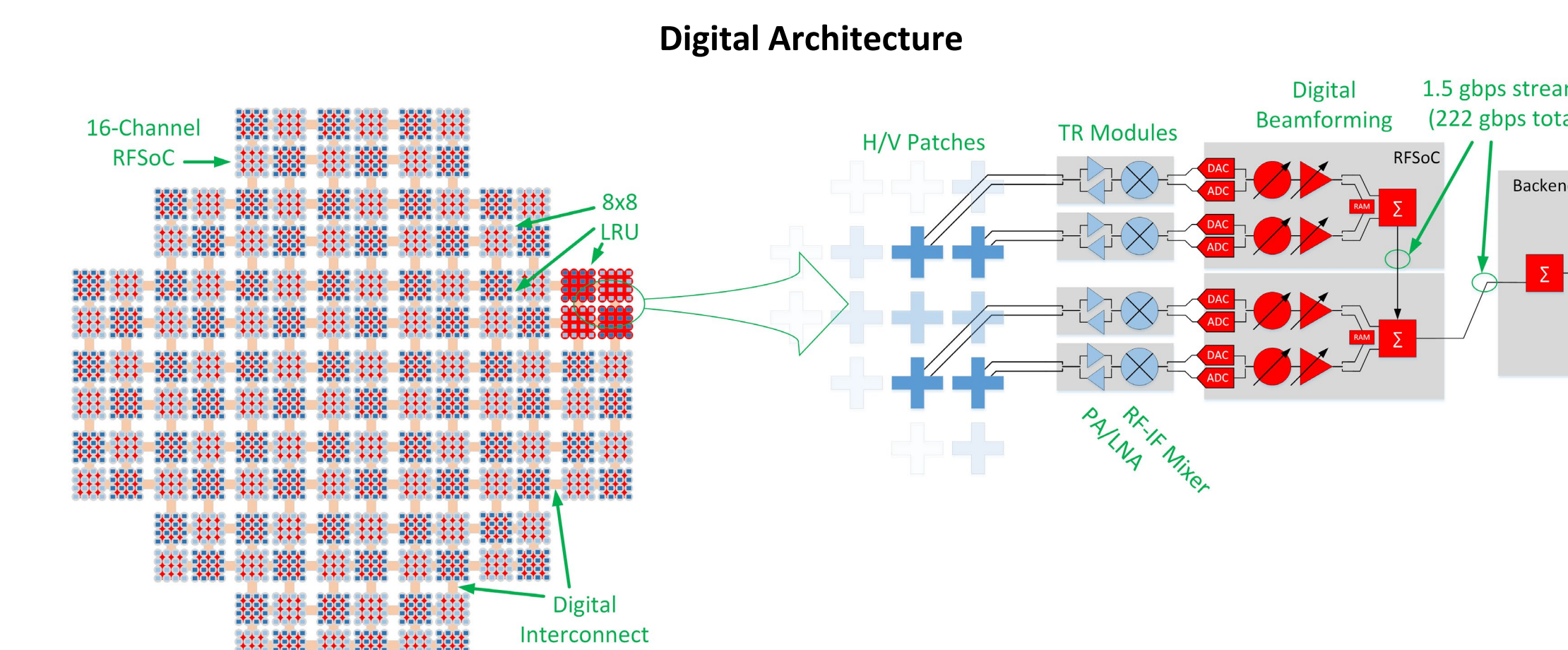
3. Beamforming Architectures



In the analog architecture, each Transmit/Receive module in the array consists of a radiating element, transmit Power Amplifier (PA), receive Low Noise Amplifier (LNA), polarization and TR switches, and a beam steering circuit - an RF phase shifter and variable attenuator. Each TR module is fed through an analog RF combiner/divider (feed network) from a single digitized channel in the receiver/exciter.



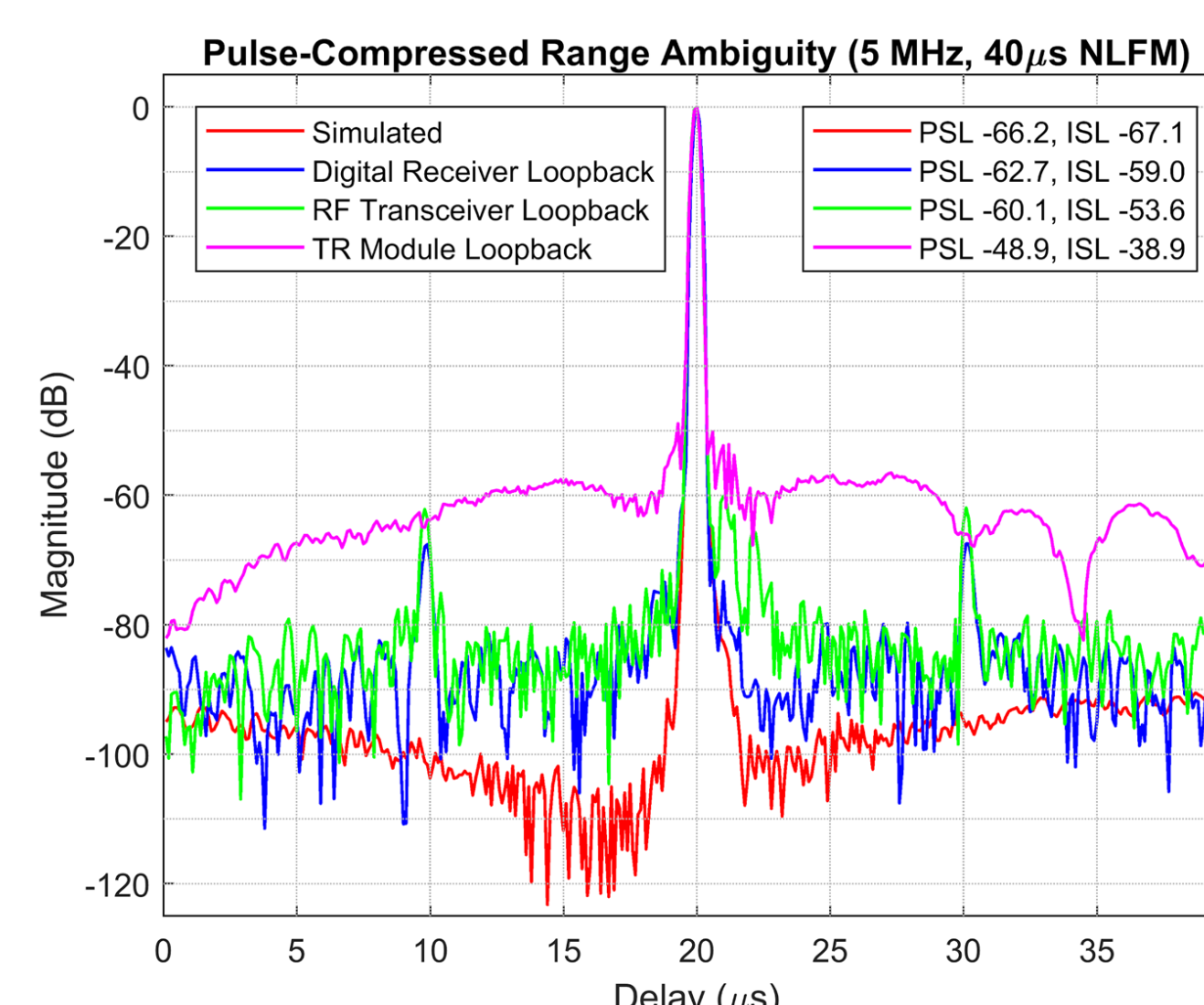
In a hybrid architecture, the T/R module design is identical to that of the analog architecture. But instead of a single feed network, the array is divided into sub-arrays. Each of the 56 rows of elements comprises one sub-array. Each sub-array is digitized separately. A single RFSoc device can digitize up to 16 channels/rows, and aggregate the data into fiber links back to the receiver/exciter.



In an Element-Level Digital architecture, the analog phase shifters and attenuators, as well as the analog feed networks, are eliminated. Each element is connected directly to a digitizer. The element gain and phase are controlled digitally, and the feed network is replaced by digital interconnect. In the proposed architecture, a 16-element tile is serviced by a 16-channel RF System on Chip (RFSoc). The RFSoc devices are interconnected in a tree topology. Each device accepts RF data from downstream device(s), and sums that data and its own into a single stream. It emits the combined stream to an upstream RFSoc, and ultimately to the receiver/exciter. By distributing the beamforming task, the data transfer burden at any single node is reduced dramatically.

4. The Need for DPD

A power amplifier is most efficient in its nonlinear (saturated) region, but this degrades signal quality. Data obtained from the APAR LRU tech demonstrator illustrates this. A prototype non-linear frequency modulated (NLFM) pulse-compressed waveform is shown under four cases - an ideal simulation, looped directly from the receiver/exciter DAC to its ADC, looped through the RF transceiver (converted from IF to C Band and back), and finally looped through the T/R module (including the power amplifier). With the PA in the loop, the range sidelobe levels increase by 11 dB (Peak SL) or 15 dB (Integrated SL). Digital Pre-distortion (DPD) can be used to mitigate the nonlinear effects of a PA.

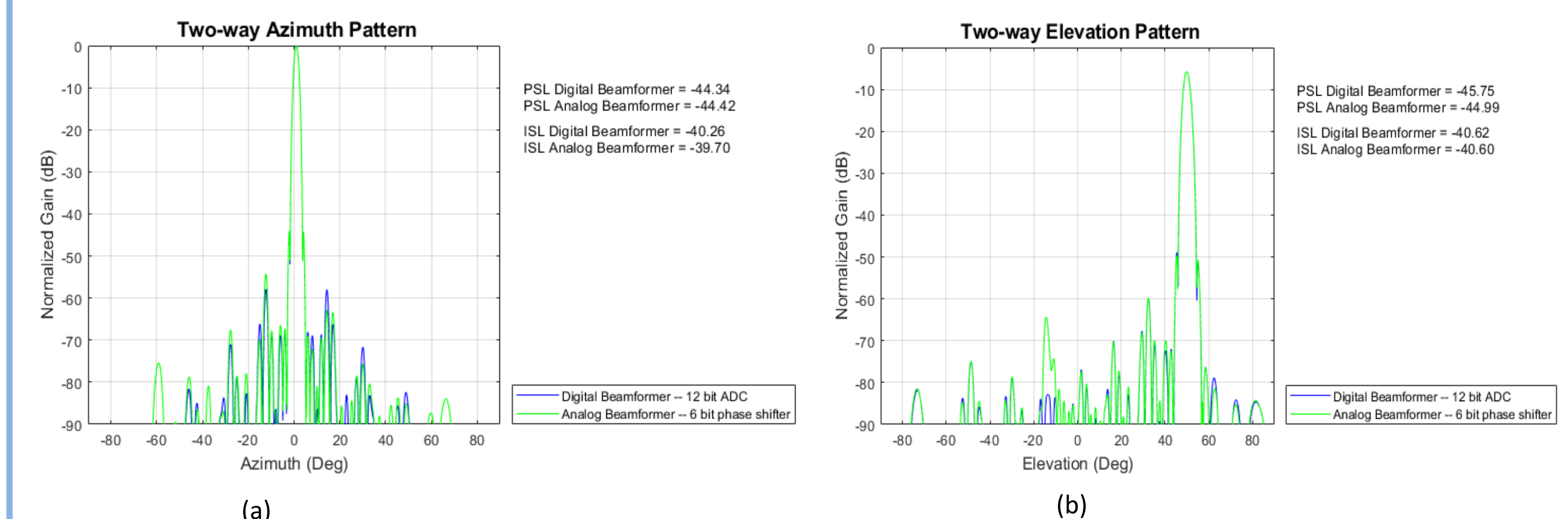


Attribute	Analog	Hybrid	Digital
Gain and phase hardware	Analog (cheapest; limited accuracy, stability, flexibility)	Analog, plus digital (per row) (Mitigates analog drawbacks at modest cost increase)	Digital (complex multiplication) (Most accurate; flexible; greatest cost and complexity)
Beam pattern	Single beam	Reconfigurable in elevation (multiple beams possible)	Arbitrarily reconfigurable (multiple beams possible)
Receiver	Single receiver chain	One chain per row	One chain per element
Dynamic Range Improvement	None	10log10(sqrt(N))	10log10(N)
Digitization of the received signals	Single weighted sum of N radiating elements	Access to sqrt(N) signals in back end (1 per row)	Access to all N elements in RFSoc; flexible output to back end
Upgradability to future beamforming techniques	Impractical (complete redesign, large NRE)	Limited improvements (via back end upgrades)	Upgradeable through firmware
Calibration/Data Quality	Performance variation of RF components difficult to track	Performance variation of RF components difficult to track	Enhanced calibration and data quality due to data at each element
Number of RFSocs	1	4	148
Compute load in Tera Ops/s	1	16	66
Aggregate ADC data rate*	12 Gb/s	672 Gb/s	28416 Gb/s
Aggregate inter-RFSoc data rate**	1.5 Gb/s	67 Gb/s	222 Gb/s/beam
Data rate to back end	1.5 Gb/s	67 Gb/s	1.5 Gb/s/beam
Power draw (AESA front end)	5.5 kW	5.5 kW	7.3 kW

Table 2. Comparison of APAR beamforming architectures

*1 GSPS, 12 bit ADC **50 MHz I/Q BW, 90 dB dynamic range Billeul 2016 and Epstein et al. 2018.

5. Effects of Quantization, Phase and Amplitude Errors



Simulation results of two way antenna pattern, including element pattern, for the beam pointing at 1° azimuth and 50° elevation scan angles. Two-way azimuth pattern, (b) two-way elevation pattern. A uniform taper is used for transmit and a 40 dB, nbar=4 Taylor taper is used on receive. Green traces assume a 6 bit phase shifter, a 3° RMS phase error and a 0.3 dB RMS amplitude error and are typical for analog beamformer. Blue traces are intended to reflect a digital beamformer and assume a 12 bit ADC. Peak sidelobe (PSL) and 1-D integrated sidelobe levels (ISL) are shown for each case.

6. Summary and Future Work

Beamforming function transforms spatial domain signals into a set of focused beams, steers the beam, and suppresses sidelobes and interference by applying a proper weighting to the multi-channel received signals. Any of the three beamforming architectures described meet the minimum requirements for the proposed APAR mission. Phase shifter resolution of 6 bits minimum is required to achieve comparable performance to digital array. RFSoc is a disruptive technology and offers potential of element level digital beamforming for an airborne AESA. Nonlinear behavior in RF hardware, phase shifters and variable attenuators among elements reduces dynamic range and data quality. Digitization of the RF frontend offers digital beam forming, configurability of PAR, improved built-in automated calibration and upgrading of the overall system with minimal impact. Increased modular and digital architecture requires order of magnitude increase in data interface and complexity of software design. For each pulse repetition interval, data throughput increases in hybrid and digital architecture. A paradigm shift in frontend data processing of digital I/Q using distributed FPGA compute resources will be required for handling high computing requirements. DPD and/or NLFM waveform modification is needed to improve range-time sidelobes.

7. References

Billeul, P. K. 2016: A new era in elemental digital beamforming for spaceborne communications phased arrays. Proc. of the IEEE, Vol. 104, No.3, 623-632.
Epstein, B., R. H. Olsson, and K. Bunch, 2018: Arrays and commercial timescales: Addressing development and upgrade costs of phased arrays. IEEE Radar Conference, Oklahoma City, OK.
Fagan, Rory, Frank C. Robey, F. C., and F., Miller, L. 2018: Phased Array Radar Cost Reduction Through the Use of Commercial RF Systems on a Chip. IEEE Radar Conference, Oklahoma City, OK.
Herd, J. S. and M.D. Conway, 2016: The evolution of modern phased array architecture. Proc. of the IEEE, Vol. 104, No.3, 519-529.
Vivekanandan, J., Lee, W.-C., Loew, E., Salazar, J. L., Grubišić, V., Moore, J., and Tsai, P.: The next generation airborne polarimetric Doppler weather radar. Geosci. Instrum. Method. Data Syst., 3, 111-126, https://doi.org/10.5194/gi-3-111-2014, 2014.
Vivekanandan, J. and Loew, E.: Airborne polarimetric Doppler weather radar: trade-offs between various engineering specifications. Geosci. Instrum. Method. Data Syst., 7, 21- 37, https://doi.org/10.5194/gi-7-21-2018, 2018.